REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add vendor, CAGE 01295 for devices 01EX and 012X. Update format. Editorial changes throughout.	90-04-09	M. A. Frye
B	Update drawing to current requirements. – drw	03-09-30	Raymond Monnin

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

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SHEET																				

REV STATUS	REV	B	B	B	B	B	B	B	B	B	B	B	B		
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12		

PMIC N/A	PREPARED BY Gary Zahn	**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43216** **http://www.dscc.dla.mil**
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY Charles E. Besore	
	APPROVED BY Michael A. Frye	MICROCIRCUIT, CMOS, 8-BIT MULTIPLYING DIGITAL TO ANALOG CONVERTER, MONOLITHIC SILICON
	DRAWING APPROVAL DATE 87-12-14	
	REVISION LEVEL B	SIZE A / CAGE CODE **67268** / **5962-87700**
		SHEET 1 OF 12

DSCC FORM 2233
APR 97

5962-E555-03

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

5962-87700	01	E	A
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device types. The device types identify the circuit function as follows:

Device type	Generic number	Circuit function
01	7524	CMOS 8-bit multiplying buffered DAC with .5 LSB
02	7524	CMOS 8-bit multiplying buffered DAC with .25 LSB
03	7524	CMOS 8-bit multiplying buffered DAC with .125 LSB

1.2.2 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
E	GDIP1-T16 and CDIP2-T16	16	Dual-in-line
2	CQCC1-N20	20	Square leadless chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

V_{DD} to GND	-0.3 V, +17 V
V_{RFB} to GND	±25 V
Digital input voltage to GND	-0.3 V to V_{DD}
V_{REF} to GND	±25 V
V_{OUT1}, V_{OUT2}, 0 to GND	-0.3 V to V_{DD}
Power dissipation (P_D):	
Up to +75°C	450 mW
Derates above +75°C	6mW/°C
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Thermal resistance, junction-to-ambient (θ_{JA})	120°C/W

1.4 Recommended operating conditions.

Ambient operating temperature range (T_A)	-55°C to +125°C
Supply voltage range (V_{DD})	+5 V to +15 V

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Mode selection table. The mode selection table shall be as specified on figure 2.

3.2.4 Write cycle timing diagram. The write cycle timing diagram shall be as specified on figure 3.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full ambient operating temperature range.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified 1/		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Resolution	RES	V_{DD} = +5 V		1, 2, 3	All	8		Bits
		V_{DD} = +15 V				8		
Relative accuracy	RA	V_{DD} = +5 V		1, 2, 3	All		±.5	LSB
		V_{DD} = +15 V		1, 2, 3	01		±.5	
				1	02		±.5	
				2, 3			±.25	
		V_{DD} = +15 V, T_A = +25°C 2/		12			±.25	
		V_{DD} = +15 V		1	03		±.5	
				2, 3			±.125	
		V_{DD} = +15 V, T_A = +25°C 2/		12			±.125	
Gain error 3/	A_E	V_{DD} = +5 V		1	All		±1.0	%FSR
				2, 3			±1.4	
		V_{DD} = +15 V		1			±0.5	
				2, 3			±0.6	
Power supply rejection	PSRR	ΔV_{DD} = ±10%	V_{DD} = +5 V	1	All		±.08	%/%
				2, 3			±.16	
			V_{DD} = +15 V	1			±.02	
				2, 3			±.04	
Output leakage current I_{OUT1}	I_{OL}	DB0-DB7 = 0 V, $\overline{WR} = \overline{CS}$ = 0 V	V_{DD} = +5 V	1	All		±50	nA
				2, 3			±400	
			V_{DD} = +15 V	1			±50	
				2, 3			±200	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified 1/		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Output leakage current I_{OUT2}	I_{OL}	DB0-DB7 = V_{DD}, $\overline{WR} = \overline{CS}$ = 0 V	V_{DD} = +5 V	1	All		±50	nA
				2, 3			±400	
			V_{DD} = +15 V	1			±50	
				2, 3			±200	
Input resistance (V_{REF} pin)	R_{IN}		V_{DD} = +5 V	1, 2, 3	All	5	20	kΩ
			V_{DD} = +15 V			5	20	
Digital input high voltage	V_{IH}		V_{DD} = +5 V	1, 2, 3	All	2.4		V
			V_{DD} = +15 V			13.5		
Digital input low voltage	V_{IL}		V_{DD} = +5 V	1, 2, 3	All		0.8	V
			V_{DD} = +15 V				1.5	
Digital input leakage current	I_{IN}	V_{IN} = 0 V or V_{DD}	V_{DD} = +5 V	1	All		±1	µA
				2, 3			±10	
			V_{DD} = +15 V	1	All		±1	
				2, 3			±10	
Supply current	I_{DD}	All digital inputs = V_{IL} or V_{IH}	V_{DD} = +5 V	1, 2, 3	All		2	mA
			V_{DD} = +15 V				2	
		All digital inputs = 0 V or V_{DD}	V_{DD} = +5 V	1	All		100	µA
				2, 3			500	
			V_{DD} = +15 V	1	All		100	
				2, 3			500	
Gain temperature coefficient	TC_{AE}	4/	V_{DD} = +5 V	1, 2, 3	All		±40	ppm/°C
			V_{DD} = +15 V				±10	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified 1/		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Feedthrough error	FT	V_{REF} = 10 V, 4/ 5/ 100 kHz sinewave DB0-DB7 = 0 V; $\overline{WR} = \overline{CS}$ = 0 V	V_{DD} = +5 V	4, 5, 6	All		50	mV p-p
			V_{DD} = +15 V				50	
Digital input capacitance	C_{IN}	V_{IN} = 0 V 6/ DB0-DB7 T_A = +25°C	V_{DD} = +5 V	4	All		5	pF
			V_{DD} = +15 V				20	
		V_{IN} = 0 V 6/ $\overline{WR}$, $\overline{CS}$ T_A = +25°C	V_{DD} = +5 V	4	All		5	
			V_{DD} = +15 V				20	
Output capacitance	C_{OUT1}	DB0-DB7 = V_{DD}; $\overline{WR} = \overline{CS}$ = 0 V T_A = +25°C 6/	V_{DD} = +5 V	4	All		120	pF
			V_{DD} = +15 V				120	
	C_{OUT2}		V_{DD} = +5 V	4	All		30	
			V_{DD} = +15 V				30	
Output capacitance	C_{OUT1}	DB0-DB7 = 0 V; $\overline{WR} = \overline{CS}$ = 0 V T_A = +25°C 6/	V_{DD} = +5 V	4	All		30	pF
			V_{DD} = +15 V				30	
	C_{OUT2}		V_{DD} = +5 V	4	All		120	
			V_{DD} = +15 V				120	
Chip select to write setup time	t_{CS}	7/	V_{DD} = +5 V	9, 10, 11	All	240		ns
			V_{DD} = +15 V			150		
Chip select to write hold time	t_{CH}	7/	V_{DD} = +5 V	9, 10, 11	All	0		ns
			V_{DD} = +15 V			0		
Write pulse width	t_{WR}	$t_{CS} \ge t_{WR}$, $t_{CH} \ge 0$ 7/	V_{DD} = +5 V	9, 10, 11	All	240		ns
			V_{DD} = +15 V			150		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified 1/		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Data setup time	t_{DS}	7/	V_{DD} = +5 V	9, 10, 11	All	170		ns
			V_{DD} = +15 V			100		
Data hold time	t_{DH}	7/	V_{DD} = +5 V	9, 10, 11	All	10		ns
			V_{DD} = +15 V			10		
Output current settling time	t_{SL}	4/, 8/	V_{DD} = +5 V	9, 10, 11	All		500	ns
			V_{DD} = +15 V				350	

1/ $V_{OUT1} = V_{OUT2} = 0$ V; $V_{REF} = +10$ V unless otherwise specified.
2/ See 4.3.1d.
3/ Measured using internal feedback R_{FB} and includes effect of leakage current and gain TC.
4/ Guaranteed, if not tested.
5/ Feedthrough error can be reduced by connecting the metal lid to ground.
6/ See 4.3.1c.
7/ Timing in accordance with figure 3.
8/ R_{OUT1} load = 100Ω, C_{EXT} = 13 pF.
$\overline{WR}$, $\overline{CS}$ = 0 V, DB0-DB7 = 0 V to V_{DD} or V_{DD} to 0 V.
Extrapolated: t_S (±1/2 LSB) = t_{PD} + 6.2 T, where T = the measured first time constant of the final RC delay.

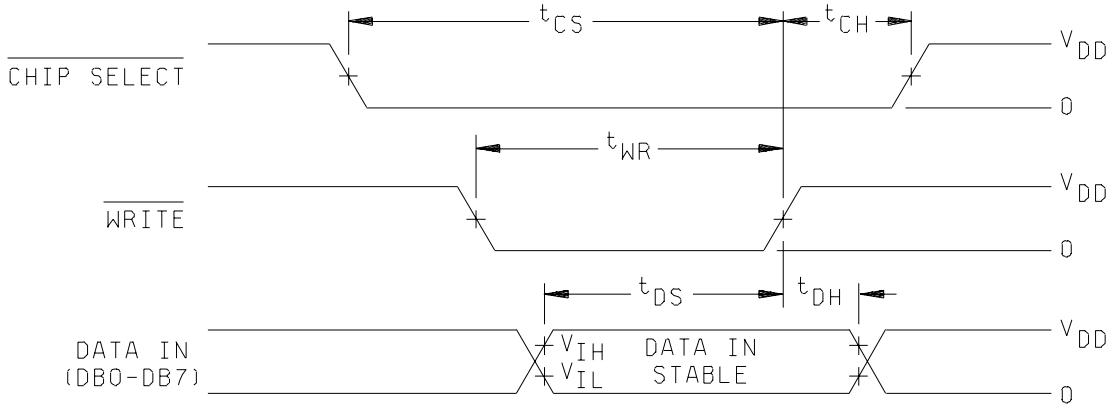
Device types	01, 02, and 03	
Case outline	E	2
Terminal number	Terminal symbol	
1	OUT 1	NC
2	OUT 2	OUT 1
3	GND	OUT 2
4	DB7 (MSB)	GND
5	DB6	DB7 (MSB)
6	DB5	NC
7	DB4	DB6
8	DB3	DB5
9	DB2	DB4
10	DB1	DB3
11	DB0 (LSB)	NC
12	$\overline{CS}$	DB2
13	$\overline{WR}$	DB1
14	V_{DD}	DB0 (LSB)
15	V_{REF}	$\overline{CS}$
16	R_{FB}	NC
17	- - -	$\overline{WR}$
18	- - -	V_{DD}
19	- - -	V_{REF}
20	- - -	R_{FB}

FIGURE 1. Terminal connections.

$\overline{CS}$	$\overline{WR}$	Mode	DAC response
L	L	Write	DAC responds to data bus (DB0 - DB7) inputs
H	X	Hold	Data bus (DB0 - DB7) is locked out
X	H	Hold	DAC holds last data present when $\overline{WR}$ or $\overline{CS}$ assumed HIGH state

L = Low state
H = High state
X = Don't care

FIGURE 2. Mode selection table.



NOTES:

1. All input signal rise and fall times measured from 10 percent to 90 percent to V_{DD}. V_{DD} = +5 V, $t_r = t_f$ = 20 ns: V_{DD} = +15 V, $t_r = t_f$ = 40 ns.
2. Timing measurement reference level is $\frac{V_{IH} + V_{IL}}{2}$.
3. $t_{DS} + t_{DH}$ is approximately constant at 145 ns minimum at +25°C, V_{DD} = +5 V and t_{WR} = 170 ns = 170 ns minimum. The devices are specified for a minimum t_{DH} of 10 ns, however, in applications where t_{DH} > 10 ns, t_{DS} may be reduced accordingly up to the limit t_{DS} = 65 ns, t_{DH} = 80 ns.

FIGURE 3. Write cycle timing diagram.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103 (see 6.6 herein). For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required in accordance with MIL-PRF-38535, appendix A.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

c. Optional subgroup 12 is used for grading and part selection at +25°C, and it is not included in PDA.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004)	1*, 2, 3, 12
Group A test requirements (method 5005)	1, 2, 3, 4, 5, 6, 9, 10**, 11**, 12
Groups C and D end-point electrical parameters (method 5005)	1

* PDA applies to subgroup 1.
** Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 7, and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance.

d. Optional subgroup 12 is used for grading and part selection at +25°C.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 03-09-30

Approved sources of supply for SMD 5962-87700 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-87700012A	24355	AD7524SE/883B
	3/	PM7524BRC/883
	3/	AD7524MFK
5962-87700012C	1ES66	MX7524SE/883B
5962-8770001EA	01295	AD7524MJ
	1ES66	MX7524SQ/883B
	3/	AD7524SQ/883B
	3/	PM7524BQ/883
5962-87700022A	24355	AD7524TE/883B
	3/	PM7524BRC/883
5962-87700022C	1ES66	MX7524TE/883B
5962-8770002EA	24355	AD7524TQ/883B
	1ES66	MX7524TQ/883B
	3/	PM7524BQ/883
5962-87700032A	24355	AD7524UE/883B
	3/	PM7524ARC/883
5962-87700032C	1ES66	MX7524UE/883B
5962-8770003EA	24355	AD7524UQ/883B
	1ES66	MX7524UQ/883B
	3/	PM7524AQ/883

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source.

Vendor CAGE number	Vendor name and address
24355	Analog Devices Rt 1 Industrial Park PO Box 9106 Norwood, MA 02062 Point of contact: Raheen Business Park Limerick, Ireland
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Ln. PO Box 660199 Dallas, TX 75243
1ES66	Maxim Integrated Products 120 San Gabriel Dr Sunnyvale, CA 94086-5125